Clean Copy Of The Currently Pending Claims Without Parenthetical Statements.

CLAIMS

We claim the following invention:

1. A signal model used in an N-NARY logic simulation, comprising:

a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

2. The model of Claim 1, wherein said logic value further comprises an integer less than or equal to 31.

3. The model of Claim 1, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

4. Canceled.

5. Canceled.

6. A method that makes a signal model used in an N-NARY logic simulation, comprising:

assigning a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

assigning a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

assigning a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

7. The method of Claim 6, wherein said logic value further comprises an integer less than or equal to 31.

8. The method of Claim 6, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

9. Canceled.

10. Canceled.

11. A method that uses a signal model used in an N-NARY logic simulation, comprising:

reading a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

reading a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled;

reading a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled; and

providing said signal value, said signal state, and said signal definition to the software-implemented simulation of the N-NARY logic design.

12. The method of Claim 11, wherein said logic value further comprises an integer less than or equal to 31.

13. The method of Claim 11, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

14. Canceled.

15. Canceled.

16. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method that uses a signal model used in an N-NARY logic simulation, comprising:

reading a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

reading a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled;

reading a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled; and

providing said signal value, said signal state, and said signal definition to the software-implemented simulation of the N-NARY logic design.

17. The program storage device of Claim 16, wherein said logic value further comprises an integer less than or equal to 31.

18. The program storage device of Claim 16, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

19. Canceled.

20. Canceled.

21. A signal modelling system used in an N-NARY logic simulation, comprising:

a signal value, said signal value further comprises the logic value of a nonbinary 1-of-N logic signal being modeled, wherein said logic value further comprises an integer greater than 1;

a signal strength, said signal strength further comprises the drive state of said nonbinary 1-of-N logic signal being modeled; and

a signal definition, said signal definition further comprises the defined or undefined status of said nonbinary 1-of-N logic signal being modeled.

22. The system of Claim 21, wherein said logic value further comprises an integer less than or equal to 31.

23. The system of Claim 21, wherein said signal strength further comprises one of the following: the high-impedance state, the weakly-driven state, the moderately-driven state, or the strongly-driven state.

24. Canceled.

25. Canceled.